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(54) **Controlling currents in laser diodes.**

(57) In an apparatus for supplying a current for driving a laser diode (1), an amount of current is supplied to the laser diode. During a read mode, a read peak current (I_{HFM}) modified by a high frequency signal (HFM) in addition to the amount of current is supplied to the laser diode, and during a write mode, a base read current (I_R) in addition to the amount of current is supplied to the laser diode so that a light output of the laser diode is equal to a base read output (P_R). The read peak current is adjusted so that a mean value of the light output of the laser diode is equal to the base read output. An automatic control is performed upon the amount of current so that the light output of the laser diode is close to the base read output.

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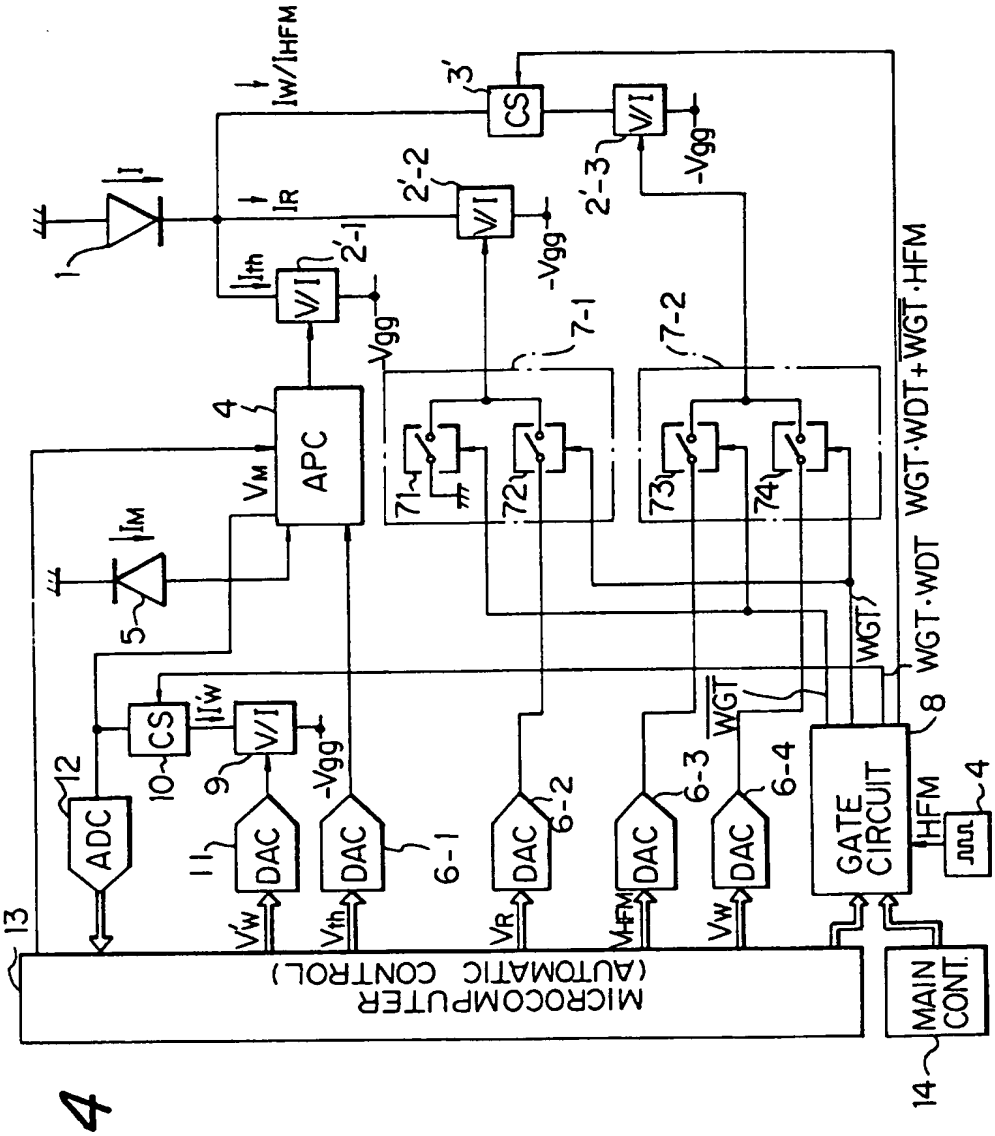

MICROCOMPUTER
(AUTOMATIC CONTROL)
MAIN CONT.
GATE CIRCUIT
ADC
DAC
APC
CS
V/I
WGT·WDT
WGT·WDT+WGT·HFM
HFM
-Vgg
Vgg

Fig. 4

The present invention relates to controlling currents in laser diodes.

In an optical storage device, apparatus may be provided for supplying a current to a laser diode of the device, to cause the laser diode to emit a light to be used when reading digital data from an optical storage medium and when writing digital date thereto.

Recently, many optical storage devices using an optical storage medium such as an optical disk, an optomagnetic disk, and an optical memory card have been developed. In such optical storage devices, a laser diode is used as a light source when carrying out a read operation and a write (erase) operation. For example, during a write mode, a laser beam is made incident on an area of a magnetic film of an optical storage medium which has been premagnetized, and as a result, that area of the magnetic film is heated, and accordingly, the direction of magnetization therein is inverted by the effect of magnetization of adjacent areas thereof. Also, during an erase mode, a laser beam is made incident on an area of the magnetic film, to heat same, and the heated area is then magnetized by using an external bias magnetic field. During a write or erase mode, a laser beam is used as the source of heat, and therefore, the driving of a laser diode for generating such heat requires a large amount of energy. On the other hand, during a read mode, when a laser beam is made incident on an area of the magnetic film, the read data is determined by a change in a plane of polarization of a reflected light, due to the Kerr effect. During a read mode, a laser diode for generating a laser beam is driven by a small amount of energy.

When the laser diode is driven by a small amount of energy, the output level of the laser diode is in a noise region, and the S/N ratio of a reproduced signal is low. Therefore, to enhance this S/N ratio, a current supplied to the laser diode can be modulated by a high frequency signal having a frequency much higher than a frequency used for recording data in the magnetic film, to enhance the peak of current supplied to the laser diode without increasing an effective output of light therefrom.

Also, to suppress fluctuations in the output of light emitted from the laser diode an automatic power control (APC) may be adopted, to bring a mean value of a light output during a read mode and a minimum light output (called a base read output) during a write mode close to a desired level.

In the above-mentioned laser diode drive system using an APC, although the desired level of the APC is not changed even when the control is transferred from a read mode to a write (or erase) mode, or vice versa, the drive current of the APC is changed, since the drive current of the laser diode, i.e. the illumination thereof during a read mode, is AC, and the current provided during a write mode for a base read output is DC. Therefore, upon a switching between a read mode and a write (or erase) mode, the control of the light output is unstable due to a delay in the response caused by a time-constant of the APC, to thus reduce a speed of an access to the optical storage medium, as later explained in detail.

It is desirable to avoid fluctuations in such an APC upon switching between a read mode and a write (or erase) mode, to thereby enhance a speed of access to an optical storage medium upon such switching.

In an embodiment of the present invention, an amount of current is supplied to a laser diode during a read mode and during a write mode, and this predetermined current is not larger than a threshold current (minimum current) which causes the laser diode to emit light. During a read mode, a read peak current modified by a high frequency signal in addition to the amount of current is supplied to the laser diode, and during a write mode, a base read current in addition to the amount of current is supplied to the laser diode, so that a light output of the laser diode is equal to a base read output. The read peak current is adjusted so that a mean value of the light output of the laser diode is equal to the base read output, and an automatic control is performed upon the amount of current so that the light output of the laser diode is close to the base read output. As a result, when the control is transferred from a read mode to a write (or erase) mode, or vice versa, since the mean value (effective value) of the light output during a read mode coincides with the light output (base read power) during a write mode, the drive current of the laser diode is not substantially changed. Therefore, the monitored output of light is not substantially changed, and thus the operation of the APC is stable. Thus, even after the control is switched, a read or write access is immediately initiated.

Note, in an erase mode, although the light output is considerably larger than the base read output, a current is absorbed by other means from a monitored light output (current) supplied to the APC. Accordingly, the operation of the APC can be acceptably stable at a switching of the control from a read mode to an erase mode or vice versa.

Reference will now be made, by way of example to the accompanying drawings, wherein:

Fig. 1 is a block circuit diagram illustrating a previously-considered apparatus for supplying a current to a laser diode;

Fig. 2 is a diagram illustrating a supplied current vs. light output characteristic of the apparatus of Fig. 1;

Figs. 3A and 3B are timing diagrams relating to operation of the apparatus of Fig. 1;

Fig. 4 is a circuit diagram illustrating apparatus for supplying a current to a laser diode according to a first embodiment of the present invention;

Fig. 5 is a logic circuit diagram of a gate circuit shown in Fig. 4;

Fig. 6 is a circuit diagram of an APC circuit shown in Fig. 1;

Fig. 7 is a circuit diagram of an example of a control current source (voltage/current conversion circuit) shown in Fig. 4;

Fig. 8 is a circuit diagram of an example of a current switch shown in Fig. 4;

Figs. 9 through 14 are flowcharts relating to operation of a microcomputer shown in Fig. 4;

Fig. 15 is a diagram showing a current supplied vs. light output characteristic of the apparatus of Fig. 4;

Fig. 16 is a circuit diagram illustrating apparatus for supplying a current to a laser diode according to a second embodiment of the present invention;

Fig. 17 is a logic circuit diagram of a gate circuit shown in Fig. 16;

Fig. 18 and 19 are flowcharts relating to operation of a microcomputer shown in Fig. 16, and

Fig. 20 is a diagram showing a current supplied vs. light output characteristic of the apparatus of Fig. 16.

In the apparatus for supplying a current shown in Fig. 1, reference numeral 1 designates a laser diode connected to two parallel control current sources (voltage to current conversion circuits) 2-1 and 2-2, which receive voltages V_1 and V_w, respectively, from a microcomputer or the like (not shown).

The control current sources 2-1 and 2-2 are switched by current switches 3-1 and 3-2, respectively.

During a read mode, the current switch 3-1 is switched by using a high frequency signal HFM supplied from a high frequency signal generator 4. In this case, the frequency of the high frequency signal HFM is much higher than a frequency used for recording data to the optical storage medium (not shown). As a result, a modified current having a read peak current I_{HFM} in addition to a threshold current I_{th} is supplied to the laser diode 1, to thereby obtain a read peak output P_{HFM}, as shown in Fig. 2.

During a write mode for data "0" (WDT = "0"), a base read current I_R in addition to the threshold current I_{th} is supplied to the laser diode 1, to thereby obtain a base read output P_R, as shown in Fig. 2.

During a write mode for data "1" (WDT = "1"), the current switch 3-2 is turned ON by a write data signal WDT, and as a result, a write current I_W is added to a current (I_{th} + I_R) flowing in the laser diode 1, to obtain a write output P_W, as shown in Fig. 2.

Also, during an erase mode, the current switch 3-1 is operated under a write mode, and the current switch 3-2 is operated under a write mode for write data "1" (WDT = "1"), and therefore, a current I_{th} + I_R + I_W is continuously supplied to the laser diode 1.

An APC circuit 4 carries out an automatic power control of a current flowing through the control current source 2-1 so that a voltage V_M corresponding to light output of the laser diode 1 monitored by a photo diode 5 is close to a voltage V_R corresponding to the base read output P_R. Thus, fluctuation of the light output of the laser diode 1 due to change of temperature, elapse of time, and the like can be compensated for.

In the Fig. 1 apparatus for supplying a current, however, when the control is transferred from a read mode to a write mode, or vice versa, the control of the output of the laser diode 1 by the APC circuit 4 may fluctuate undesirably.

For example, as shown in Fig. 3A, when the control is transferred from a read mode to a write mode for data "0", a current supplied to the laser diode 1 is changed from a modulated current I_{MOD} to a constant current I_{th} + I_R, even when the voltage V_R is constant. As a result, a light output of the laser diode 1 is fluctuated, to thereby apply noise, as a monitored output, to the APC circuit 4, and thus, the operation of the APC circuit 4 becomes unstable. Such an unstable operation state of the APC circuit 4 continues for a time T_1, depending on a time constant of the APC circuit 4, and during this time T_1 it is impossible to obtain a write access to the optical storage medium, and therefore, at worst, such a write access is initiated after one more rotation of the optical storage medium.

Similarly, as shown in Fig. 3B, when the control is transferred from a write mode for data "0" to a read mode, a current supplied to the laser diode 1 is changed from the constant current I_{th} + I_R to the modulated current I_{MOD} even when the voltage V_1 is constant. As a result, a light output of the laser diode 1 is fluctuated, to thereby apply noise, as a monitored power, to the APC circuit 4, and thus, the operation of the APC circuit 4 becomes unstable. Such an unstable operation state of the APC circuit 4 continues for a time T_2, depending on the time constant of the APC circuit 4, and during this time T_2 it is impossible to obtain a read access to the optical storage medium, and therefore, at worst, such a read access is initiated after one more rotation of the optical storage medium.

In Fig. 4, which shows a first embodiment of the present invention, three control current sources 2'-1, 2'-2, and 2'-3 are provided, and a current switch 3' is connected in series to only the control current source 2'-3.

The control current source 2'-1 is used for supplying a threshold current (minimum current) I_{th} (see Fig. 15) by which the laser diode 1 initiates the emitting of light therefrom. The APC circuit 4 is connected to only the control current source 2'-1, and therefore, an automatic power control is carried out for the threshold current I_{th} in accordance with a difference between a voltage V_{th} supplied by a digital/analog (D/A) converter 6-1 and a monitored voltage V_M supplied by the photo diode 5. The control current source 2'-2 is used for supplying a base read current I_R (see Fig. 15) to the laser diode 1 during a write mode (WGT = "1"), while not supplying a current during a read mode

($\overline{WGT}$ = "1"). For this purpose, a switching circuit 7-1 formed by two switches 71 and 72 is provided. That is, during a write mode, when a gate signal WGT (= "1") is supplied from a gate circuit 8 to the switch 72, a voltage V_R corresponding to the base read current I_R is applied by a D/A converter 6-2 to the control current source 2'-2. Note that, when a current $I_{th} + I_R$ is supplied to the laser diode 1, the light output is the base read output P_R (see Fig. 15). On the other hand, during a read mode, when a gate signal $\overline{WGT}$ (= "1") is supplied from the gate circuit 8 to the switch 71, 0 V is applied to the control current source 2'-2.

The control current source 2'-3 is used for supplying a read peak current I_{HFM} (see Fig. 15) during a read mode ($\overline{WGT}$ = "1") and supplying a write current I_W during a write mode for data "1" (WGT = WDT = "1"). For this purpose, a switching circuit 7-2 formed by two switches 73 and 74 is provided. That is, during a read mode, when the gate signal $\overline{WGT}$ (= "1") is supplied to the switch 73, a voltage V_{HFM} corresponding to the read peak current I_{HFM} is applied by a D/A converter 6-3 to the control current source 2'-3. Also, in this case, the current switch 3' is switched by the high frequency signal HFM, and therefore, the read peak current I_{HFM} is modulated by the high frequency signal HFM. Note that, when a current $I_{th} + I_{HFM}$ is supplied to the laser diode 1, the light output is the read peak output P_{HFM} (see Fig. 15). On the other hand, during a write mode for data "1", when the gate signal WGT (= "1") is supplied to the switch 74, a voltage V_W corresponding to the write current I_W is applied by a D/A converter 6-4 to the control current source 2'-3. Also, in this case, the current switch 3' is turned ON by the signal WGT·WDT (= "1"). Note that, when a current $I_{th} + I_R + I_W$ is supplied to the laser diode 1, the light output is the write output P_W (see Fig. 15).

In the APC circuit 4, the threshold voltage V_{th} by the D/A converter 6-1 is applied to one input and the monitored power voltage V_M is applied to another input. Therefore, the threshold current I_{th} flowing through the control current source 2'-1 is adjusted by the APC circuit 4 so that the monitored light output voltage V_M is brought close to the threshold voltage V_{th}. Note that a current to voltage conversion circuit is actually required to convert a current I_M flowing through the photo diode 5 to the monitored output voltage V_M at a prestage of the APC circuit 4, but such a conversion circuit is omitted for a simplification of the circuit. Also, such a conversion circuit can be included in the APC circuit 4 (see Fig. 6).

Also, a series of a control current source 9 and a current source 10 are connected in series to the photo diode 5. During a write mode for data "1", when a gate signal WGT·WDT is supplied to the current switch 10, a voltage V_W' corresponding to the write current I_W is applied by a D/A converter 11 to the control current source 9. Therefore, even when a write current I_W is added to the current flowing through the laser diode 1, an increase in the monitored output voltage V_M due to the write current I_W is absorbed by the control current source 9. Therefore, during a write mode (WGT = "1"), the monitored light output voltage V_M is maintained at a value corresponding to the base read output P_R, regardless of the write data. In this case, a voltage V_W' corresponding to the above-mentioned increase represented by a current I_W' is applied by the D/A converter 11 to the control voltage source 9, and thus, an abnormal operation of the APC circuit 4 due to the write current I_W is avoided.

Reference numeral 12 designates an A/D converter for fetching the monitored output voltage V_M. Also, in this case, note that a current to voltage conversion circuit is actually required to convert the current I_M flowing through the photo diode 5 to the monitored output voltage I_M at a prestage of the A/D converter 12, but such a conversion circuit is omitted for a simplification of the circuit.

A microcomputer 13, which is formed by a central processing unit (CPU), a read-only memory (ROM), a random access memory (RAM), and the like, is provided for controlling the various elements in Fig. 4. This microcomputer 13 is used only for an automatic adjustment of the voltages V_{th}, V_R, V_{HFM}, V_W, and W_W'.

A main controller 14 is provided for actually performing a read, write, or erase operation at the optical storage medium, after an automatic adjustment by the microcomputer 13.

Thus, the gate circuit 8 can be operated by both the microcomputer 13 and the main controller 14, as illustrated in Fig. 5.

In Fig. 5, the microcomputer 13 supplies a gate signal WGT1 during a write mode and a write data signal WDT1 to the gate circuit 8, and the main controller supplies a gate signal WGT2 during a write mode and a write data signal WDT2. Also, a high frequency signal HFM is supplied to the gate circuit 8.

The gate circuit 8 includes two OR circuits 81 and 82, an inverter 83, two AND circuits 84 and 85, and an OR circuit 86. The OR circuit 81 generates a gate signal WGT (= "1"), when the microcomputer 13 generates a gate signal WGT1 (= "1") or when the main controller 14 generates a gate signal WGT2 (= "1"). In other words, when one of the microcomputer 13 and the main controller 14 is in a write mode, the OR circuit 81 generates the gate signal WGT (= "1"). Similarly, the OR circuit 82 generates a write data signal WDT (= "1") when the microcomputer 13 generates a write data signal WDT1 (= "1"), or when the main controller 14 generates a write data signal WDT2 (= "1").

The inverter 83 inverts the output WDT of the OR circuit 81, and accordingly, generates a gate signal $\overline{WGT}$. Also, the output WDT of the OR circuit 81 is directly output.

Since the AND circuit 84 is connected to the outputs of the OR circuits 81 and 82, the AND circuit 84 generates a gate signal WGT·WDT.

Also, since the AND circuit 85 is connected to the inverter 83 and receives the high frequency signal HFM, the AND circuit 85 generates a gate signal $\overline{WGT}$·HFM.

Further, since the OR circuit 86 is connected to the outputs of the AND circuits 84 and 85, the OR circuit 86 generates a gate signal WGT·WDT + $\overline{WGT}$·HFM.

Thus, the gate signals $\overline{WGT}$, WGT, WGT·WDT, and WGT·WDT + $\overline{WGT}$·HFM are generated by the gate circuit 8.

In Fig. 6, which is a detailed circuit diagram of the APC circuit 4 of Fig. 4, the APC circuit 4 includes a differential amplifier 41 for converting a current I_M flowing through the photo diode 5 into a voltage which is already indicated by V_M, a differential amplifier 42 for generating a difference signal between the light output voltage V_M from the differential amplifier 41 and the threshold voltage V_{th} from the D/A converter 6-1, and an integrator 43. In more detail, the differential amplifier 41 is formed by an operational amplifier 411 and a variable resistor 412. That is, if the current I_M is increased, to increase a current flowing through the resistor 412, a voltage between the terminals thereof is also increased. Thus, the differential amplifier 41 generates a voltage V_M depending on the current I_M with reference to $-V_{gg1}$. Also, the differential amplifier 42 is formed by an operational amplifier 421 and resistors 421 to 424. Also, the integrator 43 is formed by an operational amplifier 431, a resistor 432, a capacitor 433, resistors 434 and 435, and switches 426 and 427 controlled by the microcomputer 13.

The switch 426 is connected in parallel to the capacitor 433, and the switch 427 is connected to a non-inverting input of the operational amplifier 431. Therefore, to release an APC, i.e., to turn OFF the APC circuit 4, the microcomputer 13 turns ON the switch 426 and turns OFF the switch 427 as illustrated in Fig. 6, so that the integrator 43 serves as a voltage buffer, thereby applying the threshold voltage V_{th} to the control current source 2'-1. On the other hand, to carry out an APC, the microcomputer 13 turns OFF the switch 426 and turns ON the switch 427, so that the integrator 43 forms an actual integrator.

In Fig. 7, which illustrates an example of the control current source such as 2'-1 of Fig. 4, the control current source 2'-1 includes an operational amplifier 701, resistors 702 through 706, and an output transistor 707. Therefore, when a voltage such as the threshold voltage V_{th} is increased, a current flowing through the resistor 705 is increased, to thus increase the base-emitter voltage V_{BE} of the output transistor 707. As a result, the current I_{th} flowing through the output transistor 707 is dependent on the threshold voltage V_{th}. In other words, the voltage V_{th} is converted to the threshold current I_{th}.

In Fig. 8, which illustrates an example of the current switches such as 3' of Fig. 4, the current switch 3' includes two NPN transistors 801 and 802 having a common emitter connected to a current source which is, in this case, the control current source 2'-3. Also, a resistor 803 is connected between a collector of the transistor 801 and a power supply such as the ground. Further, a reference voltage V_{REF} is applied to a base of the transistor 801, and a gate signal such as WGT·WDT + $\overline{WGT}$·HFM is applied to a base of the transistor 802. Therefore, if the potential of the gate signal is lower than that of the reference voltage V_{REF}, the transistor 801 is turned ON and the transistor 802 is turned OFF, so that a current I does not flow. Conversely, if the potential of the gate signal is higher than the reference voltage V_{REF}, the transistor 801 is turned OFF and the transistor 802 is turned ON, so that a current I determined by the control current source 2'-3 flows through the transistor 802.

After a power is supplied to the microcomputer 13, the microcomputer 13 carries out an automatic control, as explained below.

In Fig. 9, which is an automatic control routine carried out after the power supply to the microcomputer 13 is turned ON, at step 901, an initialization is carried out. Particularly, the contents of V_{th}, V_{HFM}, V_R, V_M, and V_W, in the RAM are cleared, and the data WGT1 and WDT1 in the RAM are reset.

At step 902, the value V_{th} (i.e., I_{th}) for the D/A converter 6-1 is determined, and at step 903, the value V_{HFM} (i.e., I_{HFM}) for the D/A converter 6-3 is determined. Also, step 904, the value V_R (i.e., I_R) for the D/A converter 6-2 is determined, and at step 905, the value V_W (i.e., I_W) for the D/A converter 6-4 is determined. Further, at step 906, the value V_W (i.e., I_W') for the D/A converter 11 is determined. Steps 902 through 907 will be explained later in more detail.

Next, at step 907, the data WGT1 and WDT1, which are set at steps 904 and 905, are reset (= "0").

Then, the routine of Fig. 9 is completed at step 908.

In Fig. 10, which is a detailed flowchart of V_{th} (I_{th}) determining step 902, the microcomputer 13 turns OFF the APC circuit 4 at step 1001, so that the threshold voltage V_{th}, which is, in this case, 0 V, is supplied from the D/A converter 6-1 directly to the control current source 2'-1. At step 1002, a monitored power voltage V_M is fetched from the A/D converter 12, and at step 1003, the monitored output voltage V_M is converted to a power P of the laser diode 1 in accordance with a predetermined function f.

At step 1004, it is determined whether or not P is larger than 0, i.e., whether or not the laser diode 1 has initiated an emitting of light therefrom. As a result, if $P \leqq 0$, the control proceeds to step 1005, which increases the value V_{th} by a definite value such as 1, and the control at steps 1002 through 1004 is then repeated. Otherwise, the control proceeds to step 1006, thus completing the routine of Fig. 10. Thus, the value V_{th}, i.e., the threshold current I_{th} is finally deter-

mined by the routine of Fig. 10, and is stored in the RAM.

In Fig. 11, which is a detailed flowchart of the V_{HFM} (I_{HFM}) determining step 903, since the data WGT1 is already reset (WGT1 = "0") and the data WGT2 of the main controller 14 is also reset (WGT2 = "0"), the value V_{HFM}, which is, in this case, 0 V, is supplied from the D/A converter 6-3 via the switch 73 to the control current source 2'-3. Also, in this case, the gate signal $WGT \cdot WDT + \overline{WGT} \cdot HFM$ of the gate circuit 8 represents HFM, and therefore, the current switch 3' is switched by the high frequency signal HFM.

First at step 1101, a mean value $\overline{P}$ of the monitored power P is cleared.

Then, at step 1102, a monitored output voltage V_M is fetched from the A/D converter 12, and at step 1103, the monitored output voltage V_M is converted into a power P of the laser diode 1 in accordance with the predetermined function f.

At step 1104, the mean value $\overline{P}$ of the monitored power P is calculated by

$$\overline{P} \leftarrow \frac{n \cdot \overline{P} + P}{n + 1}$$

where n is a positive integer such as 3, 7, 15, ... Of course, other calculation methods can be adopted. Note that, in this case, the monitored power P is an alternating current.

At step 1105, it is determined whether or not the mean value $\overline{P}$ of the monitored power P is larger than a base read output P_R, i.e., whether or not the mean value $\overline{P}$ equals the base read output P_R. As a result, if $P \leqq P_R$, the control proceeds to step 1206, which increases the value V_{HFM} by a definite value such as 1, and the control at steps 1102 through 1105 is then repeated. Otherwise, the control proceeds to step 1107, thus completing the routine of Fig. 11. Thus, the value V_{HFM}, i.e., the read peak current I_{HFM} is finally determined by the routine of Fig. 11 and is stored in the RAM.

Note that, when carrying out the routine of Fig. 11, a current $I = I_{th} + I_{HFM}$ is supplied to the laser diode 1.

In Fig. 12, which is a detailed flowchart of V_R (I_R) determining step 904, at step 1201, the gate signal WGT1 is set (WGT1 = "1"). As a result, the value V_R, which is, in this case, 0 V, is supplied from the D/A converter 6-2 via the switch 72 to the control current source 2'-2. Also, in this case, the gate signal $WGT \cdot WDT + \overline{WGT} \cdot HFM$ of the gate circuit 8 represents "0", since WGT = "1", $\overline{WDT}$ = "0", and WGT = "0". Therefore, the current switch 3' is turned OFF.

At step 1202, a monitored output voltage V_M is fetched from the A/D converter 12, and at step 1203, the monitored output voltage V_M is converted into a power P of the laser diode 1 in accordance with the predetermined function f.

At step 1204, it is determined whether or not P is larger than P_R, i.e., whether or not the light power P equals the base read output P_R. As a result, if $P \leqq P_R$, the control proceeds to step 1205 which increases the value V_R by a definite value such as 1, and the control at steps 1202 through 1204 is then repeated. Otherwise, the control proceeds to step 1206, thus completing the routine of Fig. 12. Thus, the value V_R for the base read output P_R is finally determined by the routine of Fig. 12, and is stored in the RAM.

Note that, when carrying out the routine of Fig. 12, a current $I = I_{th} + I_R$ is supplied to the laser diode 1.

In Fig. 13, which is a detailed flowchart of the V_W (I_W) determining step 905, at step 1301, the data signal WDT1 is set (W1) T1 = "1"). As a result, the gate signal $WGT \cdot WDT + WGT \cdot HFM$ of the gate circuit 8 represents "1", since WGT = "1", WDT = "1", and $\overline{WGT}$ = "0". Therefore, the current switch 3" is turned ON. Also, in this case, since the gate signal WGT of the gate circuit 8 is "1", the value V_W, which is, in this case, 0 V, is supplied from the D/A converter 6-4 via the switch 74 to the control current source 2'-3.

At step 1302, a monitored output voltage V_M is fetched from the A/D converter 12, and at step 1403, the monitored output voltage V_M is converted into a power P of the laser diode 1 in accordance with the predetermined function f.

At step 1304, it is determined whether or not P is larger than P_W, i.e., whether or not the light power P reaches the write power P_W. As a result, if $P \leqq P_W$, the control proceeds to step 1205 which increases the value V_R by a definite value such as 1, and the control at steps 1402 through 1404 is then repeated. Otherwise, the control proceeds to step 1406, thus completing the routine of Fig. 13. Thus, the value V_W for the write output P_W is finally determined by the routine of Fig. 13, and is stored in the RAM.

Note that, when carrying out the routine of Fig. 13, a current $I = I_{th} + I_R + I_W$ is supplied to the laser diode 1.

In Fig. 14, which is a detailed flowchart of V_W' (I_W') determining step 906, at step 1401, the microcomputer 13 turns ON the APC circuit 4.

At step 1402, a monitored output voltage V_M is fetched from the A/D converter 12, and at step 1403, the monitored output voltage V_M is converted into a power P of the laser diode 1 in accordance with the predetermined function f.

At step 1404, it is determined whether or not P is larger than P_R, i.e., whether or not the light power P is equal to the base read output P_R. As a result, if $P \leqq P_R$, the control proceeds to step 1405 which increases the value V_W' by a definite value such as 1, and the control at steps 1402 through 1404 is then repeated. Otherwise, the control proceeds to step 1406, thus completing the routine of Fig. 14. Thus, the value V_W' for an increased power due to the write current I_W is finally determined by the routine of Fig. 14, and is stored in the RAM.

Note that, when carrying out the routine of Fig. 14, a current $I = I_{th} + I_R + I_W$ is supplied to the laser diode

1.

The operation of the main controller 14 of Fig. 4 will be explained with reference to Fig. 15 which shows a current I supplied to a light power P characteristic of the current supplying apparatus of Fig. 4.

During a read mode, the main controller 14 generates a gate signal WGT2 (= "0"), and accordingly, the gate circuit 8 generates a first gate signal $\overline{WGT}$ (= "0"), a second gate signal WGT (= "0"), a third gate signal WGT·WDT (= "0"), and a fourth gate signal WGT·HFM + WGT·WDT = HFM. By the first gate signal $\overline{WGT}$ and the second gate signal WGT, the switches 71 and 73 are turned ON, and the switches 72 and 74 are turned OFF. Therefore, 0 V is applied to the control current source 2'-2, and the read peak voltage V_R is applied to the control current source 2'-3. By the third gate signal WGT·WDT (= "0"), the current switch 10 is turned OFF, and therefore, a monitored output current I_M is not absorbed in the control current source 9. By the fourth gate signal HFM, the current switch 3' is switched by a frequency of the high frequency signal HFM. As a result, a current $I = I_{th}$ and a current $I = I_{th} + I_{HFM}$ is alternatingly supplied to the laser diode 1, and accordingly, a read peak output P_{HFM} alternatingly appears as shown in Fig. 15. In this case, a mean value $\overline{P}$ of a light power P of is brought close to the base read output P_R by an automatic power control of the APC circuit 4, as shown in Fig. 15.

During a write mode for data "0", the main controller 14 generates a gate signal WGT2 (= "1") and a data signal WDT2 (= "0"), and the gate circuit 8 generates a first gate signal $\overline{WGT}$ (= "0"), a second gate signal WGT (= "1"), a third gate signal WGT·WDT (= "0"), and a fourth gate signal $\overline{WGT}$·HFM + WGT·WDT (= "0"). By the first gate signal $\overline{WGT}$ and the second gate signal WGT, the switches 72 and 74 are turned ON, and the switches 71 and 73 are turned OFF. Therefore, the voltage V_R is applied to the control current source 2'-2, and the voltage V_W is applied to the control current source 2'-3. By the third gate signal WGT·WDT (= "0"), the current switch 10 is turned OFF, and therefore, a monitored output current I_M is not absorbed in the control current source 9. By the fourth gate signal $\overline{WGT}$·HFM + WGT·WDT (= "0"), the current switch 3' is turned OFF. As a result, a current $I = I_{th} + I_R$ is supplied to the laser diode 1, and accordingly, the base read output P_R appears as shown in Fig. 15. In this case, a light power P_1 is brought close to the base read output P_R by an automatic power control of the APC circuit 4, as shown in Fig. 15.

During a write mode for data 1", the main controller 14 generates a gate signal WGT2 (= "1") and a data signal WDT2 (= "1"), and the gate circuit 8 generates a first gate signal $\overline{WGT}$ (= "0"), a second gate signal WGT (= "1"), a third gate signal WGT·WDT (= "1"), and a fourth gate signal $\overline{WGT}$·HFM + WGT·WDT (= "1"). By the first gate signal $\overline{WGT}$ and the second gate signal WGT, the switches 72 and 74 are turned ON, and the switches 71 and 73 are turned OFF. Therefore, the voltage V_R is applied to the control current source 2'-2, and the voltage V_W is applied to the control current source 2'-3. By the third gate signal WGT·WDT (= "1"), the current switch 10 is turned ON, and therefore, a monitored output current I_M is absorbed in the control current source 9. By the fourth gate signal $\overline{WGT}$·HFM + WGT·WDT (= "1"), the current switch 3' is turned ON. As a result, a current $I = I_{th} + I_R + I_W$ is supplied to the laser diode 1, and accordingly, the write output P_W appears as shown in Fig. 15. In this case, a light power P_2, which is equal to the write output P_W minus ΔP corresponding to the write current I_W, is brought close to the base read output P_R by an automatic power control of the APC circuit 4, as shown in Fig. 15.

During an erase mode, the main controller 14 always generates a gate signal WGT2 (= "1") and a data signal WDT2 (= "1"), in the same way as during a write mode for data "1". Therefore, a current $I = I_{th} + I_R + I_W$ is supplied to the laser diode 1, and accordingly, the write output P_W also appears. Also, in this case, a light power P_2, which is equal to the write output P_W minus ΔP corresponding to the write current I_W, is brought close to the based read output P_R by an automatic power control of the APC circuit 4.

As shown in Fig. 15, the following condition is satisfied:

$$I_R < I_{HFM} < I_R + I_W.$$

Also, as shown in Fig. 15, the mean value $\overline{P}$ of the light power P during a read mode is coincided with the light power P_1 and P_2 during a write mode. Note that both the light power $\overline{P}$ and P_1 (P_2) are brought close to the base read output P_R. Therefore, at a switching between a read mode and a write mode (also erase mode), an automatic power control by the APC circuit 4 is hardly fluctuated.

In Fig. 16, which relates to a second embodiment of the present invention, three control current sources 2'-4, 2'-5, and 2'-6 are provided instead of the control current sources 2'-2 and 2'-3 of Fig. 4, and current switches 3'-1, 3'-2, and 3'-3 are connected in series to the control current sources 2'-4, 2'-5, and 2'-6, respectively. Also, the switching circuit 7-1 and 7-2 and the D/A converter 6-2 of Fig. 4 are not provided, and a D/A converter 6-5 is added.

The control current source 2'-4 is used for supplying the read peak current I_{HFM} to the laser diode 1 during a read mode. Therefore, the read peak voltage V_{HFM} is applied by the D/A converter 6-3 to the control current source 2'-4 and the current switch 3'-1 is turned ON in accordance with the high frequency signal HFM during a read mode ($\overline{WGT}$ = "1"). However, the current switch 3'-1 is turned ON even during a write mode (WGT = "1").

The control current source 2'-5 is used for supplying the write current I_W during a write mode for data "1". Therefore, the write voltage V_W for the write cur-

rent I_W is applied by the D/A converter 6-4 to the control current source 2'-5, and the current switch 3'-2 is turned ON during a write mode for data "1" (WGT = WDT = "1").

The control current source 2'-6 is used for supply a correction current I_S to the control current sources 2'-1, 2'-4, and 2'-5, i.e., for subtracting the correction current I_S from a current I flowing through the laser diode I during a write mode. Therefore, a correction voltage V_S is applied by the D/A converter 6-5 to the control current source 3'-3, and the current switch 2'-6 is turned ON during a write mode (WGT = "1").

A gate circuit 8' is obtained by modifying the gate circuit 8 of Fig. 4.

In Fig. 17, which is a detailed circuit diagram of the gate circuit 8' of Fig. 16, an OR circuit 86 is different from the OR circuit 86 of Fig. 5. That is, the OR circuit 86' is connected to the outputs of the OR circuit 81 and the AND circuit 85. Therefore, the OR circuit 86' generates a gate signal WGT + $\overline{WGT}$·HFM. Also, the gate circuit 8' does not generate the gate signal $\overline{WGT}$.

An automatic control by the microcomputer 13 in Fig. 16 is illustrated in Fig. 18. That is, steps 1801 and 1802 are provided instead of steps 901 and 902 of Fig. 9. At step 1801, the value V_S instead of the value V_R is cleared. Also, at step 1802, the value V_S for the correction current I_S for the D/A converter 6-5 is determined.

In Fig. 19, which is a detailed flowchart of the V_S (I_S) determining step 1802, at step 1901, the gate signal WGT1 is set (WGT1 = "1"), i.e., the gate signal WGT is set (WGT = "1"). As a result, the current switch 3'-2 is turned ON, and accordingly, the read peak current I_{HFM} is supplied to the laser diode 1. Also, the current switch 3'-3 is turned ON, and accordingly, a correction current I_S corresponding to the correction voltage V_S which is, in this case, 0 V, flows through the control current source 2'-6. Also, in this case, the gate signal WGT·WDT of the gate circuit 8' represents "0", since WDT = "1". Thus, the current switch 3'-2 is turned OFF. Therefore, a current $I = I_{th} + I_{HFM} - I_S$ is supplied to the laser diode 1. Here $I_S = 0$.

At step 1902, a monitored output voltage V_M is fetched from the A/D converter 12, and at step 1903, the monitored output voltage V_M is converted into a power P of the laser diode 1 in accordance with the predetermined function f.

At step 1904, it is determined whether or not P is smaller than P_R, i.e., whether or not the light power P reaches the base read output P_R. As a result, if $P \geqq P_R$, the control proceeds to step 1905 which increases the value V_S by a definite value such as 1, and the control at steps 1902 through 1904 is then repeated. Otherwise, the control proceeds to step 1906, thus completing the routine of Fig. 19. Thus, the value V_S for the correction current I_S is finally determined by the routine of Fig. 19, and is stored in the RAM.

Also, note that, when carrying out the V_W (I_W) determining step 905 and the V_W' (I_W') determining step 906, a current $I = I_{th} + I_{HFM} - I_S + I_W$ is supplied to the laser diode 1.

The operation of the main controller 14 of Fig. 16 will be explained with reference to Fig. 20, which shows a current I supplied to a light power P characteristic of the current supplying apparatus of Fig. 16.

During a read mode, the main controller 14 generates a gate signal WGT2 (= "0"), and accordingly, the gate circuit 8' generates a first gate signal WGT (= "0"), a second gate signal WGT·WDT (= "0"), and a third gate signal WGT + $\overline{WGT}$·HFM = HFM. By the first gate signal WGT (= "0"), the current switch 3'-3 is turned OFF, and accordingly, the correction current I_S does not flow. By the second gate signal WGT·WDT (= "0"), the current switch 3'-2 and 10 are turned OFF, and accordingly, the write current I_W and the current I_W' do not flow.

By the third gate signal HFM, the current switch 3'-1 is switched by a frequency of the high frequency signal HFM. As a result, a current $I = I_{th}$ and a current $I = I_{th} + I_{HFM}$ is alternatingly supplied to the laser diode 1, and accordingly, a read peak output P_{HFM} alternatingly appears as shown in Fig. 20. In this case, a mean value $\overline{P}$ of a light power P of is brought close to the base read output P_R by an automatic power control of the APC circuit 4, as shown in Fig. 20.

During a write mode for data "0", the main controller 14 generates a gate signal WGT2 (= "1") and a data signal WDT2 (= "0"), and the gate circuit 8' generates a first gate signal WGT (= "1"), a second gate signal WGT·WDT (= "0"), and a third gate signal WGT + $\overline{WGT}$·HFM (= "1"). By the first gate signal WGT (= "1"), the current switch 3'-3 is turned ON, and accordingly, the correction current I_S flows through the control current source 2'-6. By the second gate signal WGT·WDT (= "0"), the current switches 3'-2 and 10 are turned OFF, and accordingly, the write current I_W and the current I_W' do not flow. As a result, a current $I = I_{th} + I_{HFM} - I_S$ is supplied to the laser diode 1, and accordingly, the base read output P_R appears as shown in Fig. 20. In this case, a light power P_1 is brought close to the base read output P_R by an automatic power control of the APC circuit 4, as shown in Fig. 20.

During a write mode for data "1", the main controller 14 generates a gate signal WGT2 (= "1") and a data signal WDT2 (= "1"), and the gate circuit 8' generates a first gate signal WGT (= "1"), a second gate signal WGT·WDT (= "1"), and a third gate signal WGT + $\overline{WGT}$·HFM (= "1"). By the first gate signal WGT (= "1"), the current switch 3'-3 is turned ON, and accordingly, the correction current I_S flows through the control current source 2'-6. By the second gate signal WGT·WDT (= "1"), the current switches 3'-2 and 10 are turned ON, and accordingly, the write current I_W

is supplied to the laser diode 1 and the current I_W' in the monitored output current I_M is absorbed by the control current source 9. By the third gate signal WGT + $\overline{WGT}$·HFM (= "1"), the current switch 3'-1 is turned ON, and accordingly, the write current I_W is supplied to the laser diode 1. As a result, a current $I = I_{th} + I_{HFM} - I_S + I_W$ is supplied to the laser diode 1, and accordingly, the write output P_W appears as shown in Fig. 20. In this case, a light power P2 , which is equal to the light power P_W minus ΔP corresponding to the write current I_W , is brought close to the based read output P_R by an automatic power control of the APC circuit 4, as shown in Fig. 20.

During an erase mode, the main controller 14 always generates a gate signal WGT2 (= "1") and a data signal WDT2 (= "1"), in the same way as during a write mode for data "1". Therefore, a current $I = I_{th} + I_{HFM} - I_S + I_W$ is supplied to the laser diode 1, and accordingly, the write output P_W also appears. Also, in this case, a light power P_2 , which is equal to the light power P_W minus ΔP corresponding to the write current I_W , is brought close to the base read output P_R by an automatic power control of the APC circuit 4.

As shown in Fig. 20, the following condition is satisfied:

$$I_{HFM} - I_S < I_{HFM} < I_{HFM} - I_S + I_W.$$

Also, as shown in Fig. 20, the mean value $\overline{P}$ of the light power P during a read mode is coincided with the light power P_1 and P_2 during a write mode. Note that both the light power $\overline{P}$ and P_1 (P_2) are brought close to the base read output P_R. Therefore, at a switching between a read mode and a write mode (also erase mode), an automatic power control by the APC circuit 4 is hardly fluctuated.

In the above-mentioned embodiments, although the value I_{th} is determined by a threshold current of the laser diode 1 which initiates an emitting of light therefrom, the value I_{th} can be smaller than such a threshold current.

In an apparatus embodying the present invention, fluctuations of an APC at a switching between a read mode and a write mode (or erase mode) can be avoided, to increase an access speed to an optical storage medium.

Thus, an embodiment of the present invention can provide an apparatus supplying a current to a laser diode emitting light onto an optical storage medium, to thereby read digital data therefrom and to write digital data thereto, comprising light power monitoring means for monitoring a light power of light emitted from said laser diode; a first current supply means for supplying a first current to said laser diode; a second current supply means for supplying a second current to said laser diode during a write mode; a third current supply means for supplying a third current to said laser diode during a read mode, said third current modulated with a high frequency signal and said first current being supplied to said laser diode so that a mean value of the monitored light power is equal to a base read power; a fourth current supply means for supplying a fourth current to said laser diode during the write mode; a switching means for turning ON and OFF said fourth current in accordance with write data during the write mode; and automatic power control means for controlling said first current in accordance with the monitored light power.

A further embodiment of the present invention can provide a current supplying apparatus for supplying a current to a laser diode for emitting light to an optical storage medium, to thereby read digital data therefrom and to write digital data thereto, comprising light power monitoring means for monitoring a light power of light emitted from said laser diode; a first current supply means for supplying a first current to said laser diode; a second current supply means for supplying a second current to said laser diode during a read mode and a write mode; said third current modulated with a high frequency signal and said first current being supplied to said laser diode so that a mean value of the monitored light power is equal to a base read power; current absorbing means for absorbing a correction current from said second current during the write mode; a third current supply means for supplying a third current to said laser diode during the write mode; a switching means for turning ON and OFF said third current in accordance with write data during the write mode; and automatic power control means for controlling said first current in accordance with the monitored light power.

Claims

1. An apparatus supplying a current (I) to a laser diode (1) emitting light onto an optical storage medium, to thereby read digital data therefrom and to write digital data thereto, comprising:

light power monitoring means (5) for monitoring a light power of light emitted from said laser diode;

a first current supply means (2'-1, 6-1) for supplying a first current to said laser diode;

a second current supply means (2'-2, 6-2, 72) for supplying a second current (I_R) to said laser diode during a write mode (WGT = "1");

a third current supply means (2'-3, 3', 6-3, 73) for supplying a third current (I_{HFM}) to said laser diode during a read mode (WGT = "0"), said third current modulated with a high frequency signal (HFM) and said first current being supplied to said laser diode so that a mean value of the monitored light power is equal to a base read power (P_R);

a fourth current supply means (2'-3, 3', 6-4, 74) for supplying a fourth current (I_W) to said laser diode during the fourth mode;

a switching means (3', 8) for turning ON and OFF said fourth current in accordance with write data (WDT) during the write mode; and

automatic power control means (4) for controlling said first current in accordance with the monitored high power.

2. An apparatus as set forth in claim 1, wherein said first current being not larger than a threshold current (I_{th}) which is a minimum current at which said laser diode is able to emit light,

3. An apparatus as set forth in claim 1, wherein a sum of said first current and said second current being a value between said threshold current and said third current and being supplied to said laser diode so that the monitored light power is equal to a base read power (P_R).

4. An apparatus as set forth in claim 1, wherein a sum of said first current and said third current being larger than said threshold current and being suppoied to said laser diode so that the monitored light power is equal to a read peak power (P_{HFM}).

5. An apparatus as set forth in claim 1, wherein a sum of said first current and said fourth current is larger than the sum of said first current and said third current and being supplied to said laser diode so that the monitored light power is equal to a write power (P_W).

6. An apparatus as set forth in claim 1, further comprising;

a high frequency signal generating means (4) for generating said high frequency signal (HFM);

a switching means (3', 8) for modulating said third current with said high frequency signal during the read mode;

means for adjusting said third current (I_{HFM}) so that a means value of the monitored light power is equal to the base read power (P_R) when the modulated read peak current and said predetermined current are supplied to said laser diode.

7. An apparatus as set forth in claim 1, further comprising means (8) for continuously operating said third and fourth current supplying means so that the monitored light power is always equal to the write power (P_W).

8. An apparatus as set forth in claim 1, further comprising means (13) for operating said automatic power control means during the read mode and during the write mode for a lower power data (WDT="0").

9. An apparatus as set forth in claim 1, further comprising:

means (13) for operating said automatic power control means during the read mode and during the write mode; and

current absorbing means (9 - 11), connected between said light power monitoring means and said automatic power control means, for absorbing a power from the monitored light power when said fourth current is supplied to said laser diode, said power corresponding to a difference between said write power (P_W) and said base read power (P_R).

10. A current supplying apparatus for supplying a current (I) to a laser diode (1) for emitting light to an optical storage medium, to thereby read digital data therefrom and to write digital data thereto, comprising:

light power monitoring means (5) for monitoring a light power of light emitted from said laser diode;

a first current supply means (2'-1, 6-1) for supplying a first current to said laser diode;

a second current supply means (2'-4, 3'-1, 6-3) for supplying a second current (I_{HFM}) to said laser diode during a read mode (WGT = "0") and a write mode (WGT = "1"); said third current modulated with a high frequency signal (HFM) and said first current being supplied to said laser diode so that a mean value of the monitored light power is equal to a base read power (P_R);

current absorbing means (2'-6, 3'-3) for absorbing a correction current (I_S) from said second current during the write mode;

a third current supply means (2'-5, 3'-2, 6-4) for supplying a third current (I_W) to said laser diode during the write mode;

a switching means (3'-1, 8') for turning ON and OFF said write current in accordance with write data (WDT) during the write mode; and

automatic power control means (4) for controlling said first current in accordance with the monitored light power.

11. An apparatus as set forth in claim 10, wherein said first current being not larger than a threshold current (I_{th}) which is a minimum current at which said laser diode is able to emit light.

12. An apparatus as set forth in claim 1, wherein a sum of said first current and said second current being larger than said threshed current and being supplied to said laser diode so that the monitored light power is equal to a read peak power (P_{HFM}).

13. An apparatus as set forth in claim 10, wherein a sum of said first current and said second current

minus said correction current being larger than said threshold current and being supplied to said laser diode so that the monitored light power is equal to a base read power (P_R).

14. An apparatus as set forth in claim 10, wherein a sum of said first current and said third is larger than the sum of said first current and said second current and being supplied to said laser diode so that the monitored light power is equal to a write power (P_W);

15. An apparatus as set forth in claim 10, further comprising;

a high frequency signal generating means (4) for generating said high frequency signal (HMF);

a switching means (3'-2 , 8') for modulating said third current with said high frequency signal during the read mode;

means for adjusting said second current (I_{HMF}) so that a means value of the monitored light power is equal to the base read power (P_R) when the modulated second current and said first current are supplied to said laser diode.

16. An apparatus as set forth in claim 10, further comprising means (8') for continuously operating said second and third current supplying means, and said current absorbing means so that the monitored light power is always equal to the write power (P_W).

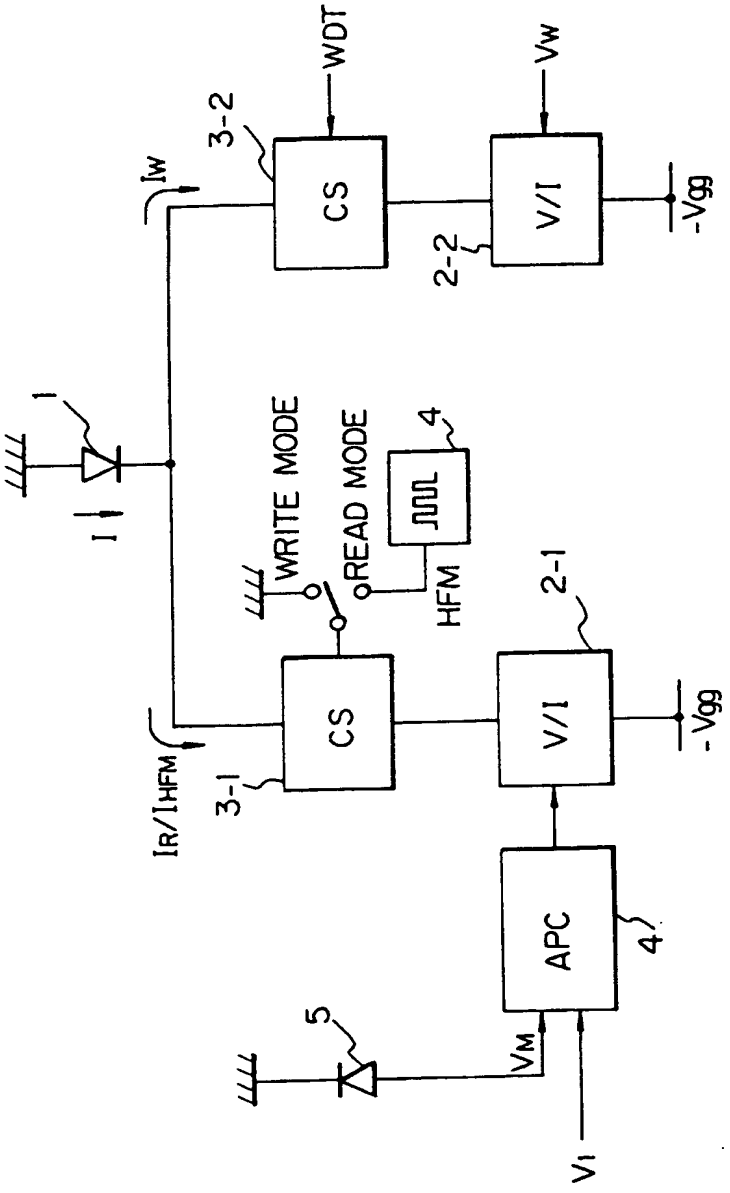
17. An apparatus as set forth in claim 10, further comprising means (13) for operating said automatic power control means during the read mode and during the write mode for a lower power data (WTD="0").

18. An apparatus as set forth in claim 10, further comprising:

means (13) for operating said automatic power control means during the read mode and during the write mode; and

another current absorbing means (9 - 11), connected between said light power monitoring means and said automatic power control means, for absorbing a power from the monitored light power when said third current is supplied to said laser diode, said power corresponding to a difference between said write power (P_W) and said base read power (P_R).

Fig. 1


WDT
Vw
3-2
CS
V/I
-Vgg
Iw
2-2
1
WRITE MODE
READ MODE
4
HFM
2-1
CS
V/I
-Vgg
IR/IHFM
3-1
APC
4
5
VM
VI

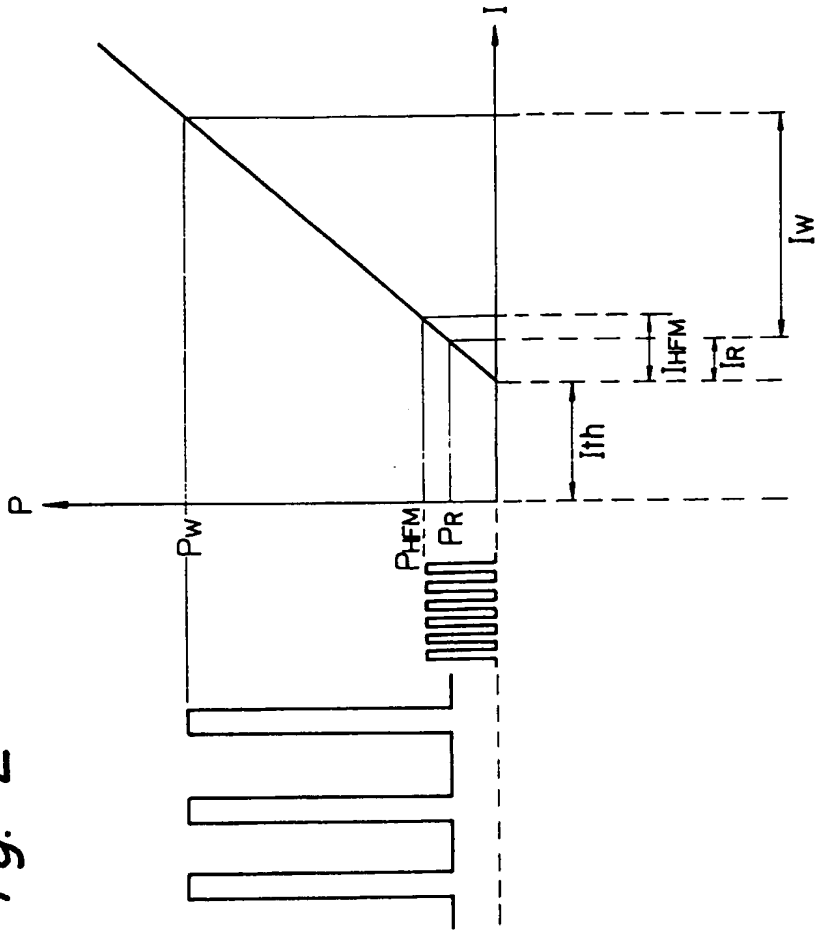


Fig. 2

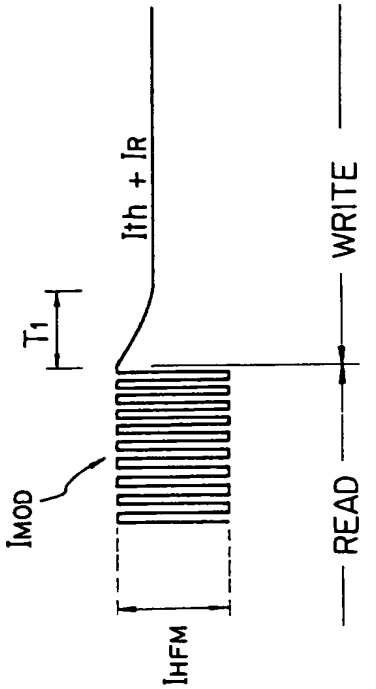


Fig. 3A

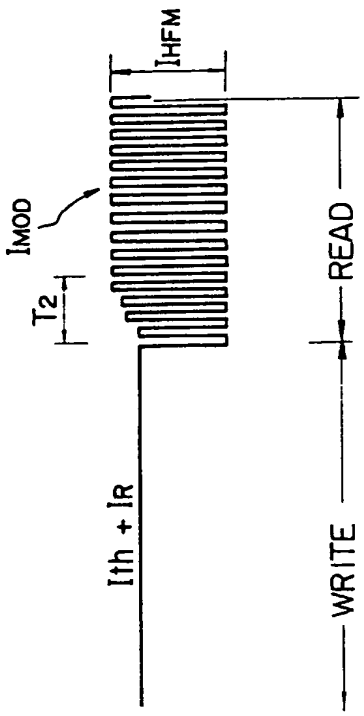


Fig. 3B

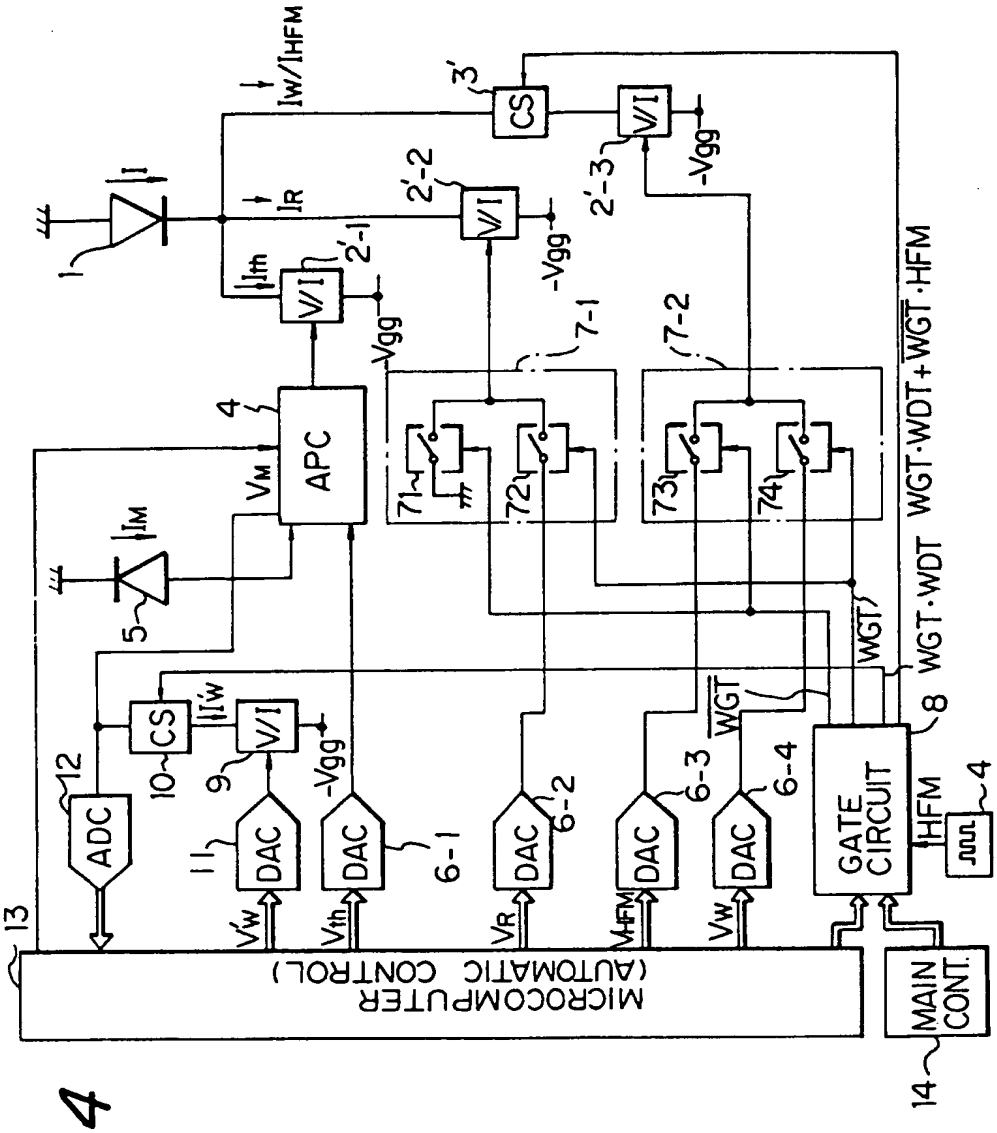

MICROCOMPUTER
(AUTOMATIC CONTROL)
MAIN CONT.
ADC
DAC
APC
CS
V/I
GATE CIRCUIT
HFM
WGT·WDT
WGT·WDT+WGT·HFM
-Vgg

Fig. 4

Fig. 5

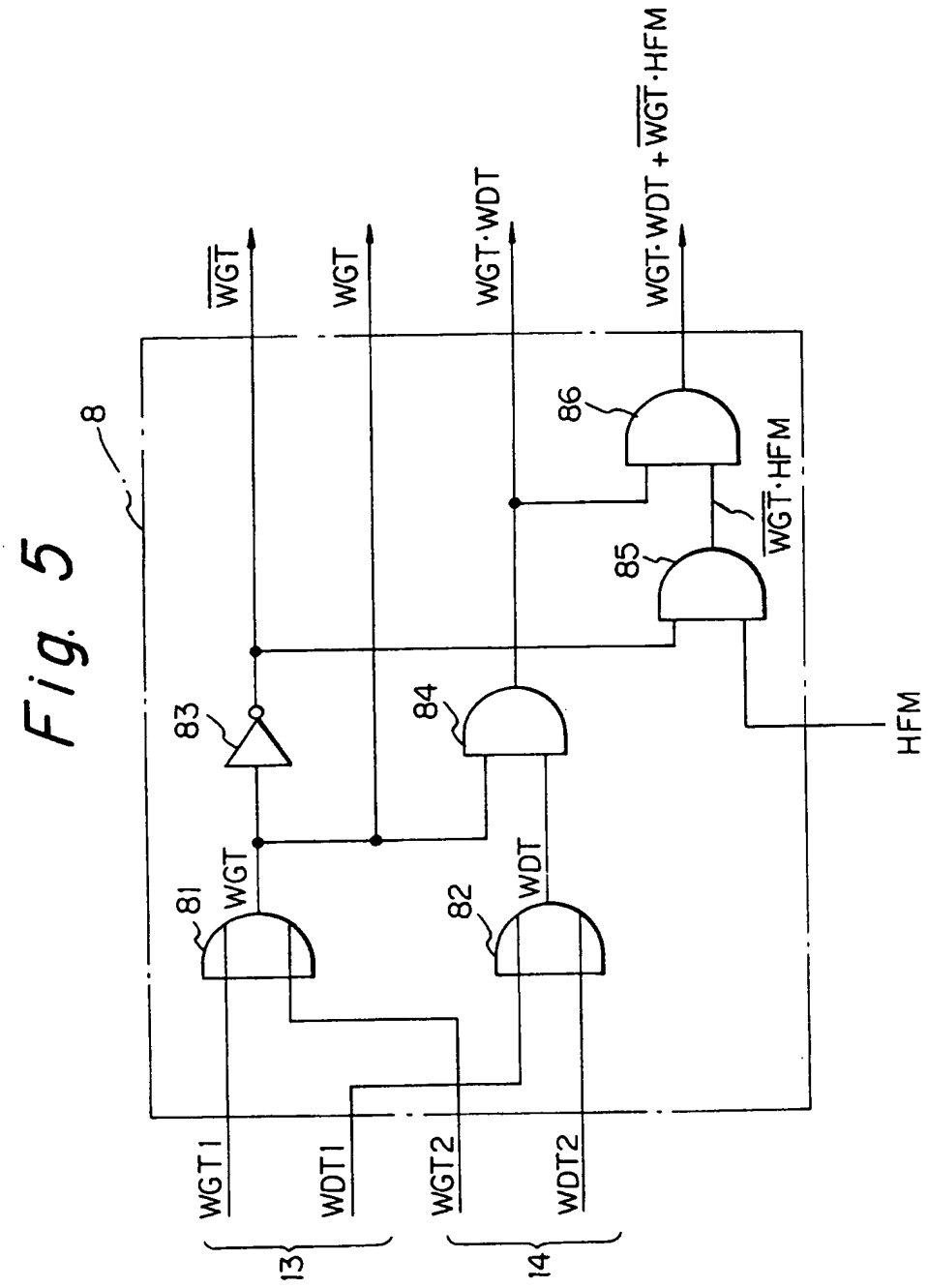

8
$\overline{WGT}$
WGT
WGT·WDT
WGT·WDT + $\overline{WGT}$·HFM
86
$\overline{WGT}$·HFM
85
HFM
83
84
81
WGT
82
WDT
WGT1
WDT1
WGT2
WDT2
13
14

Fig. 6

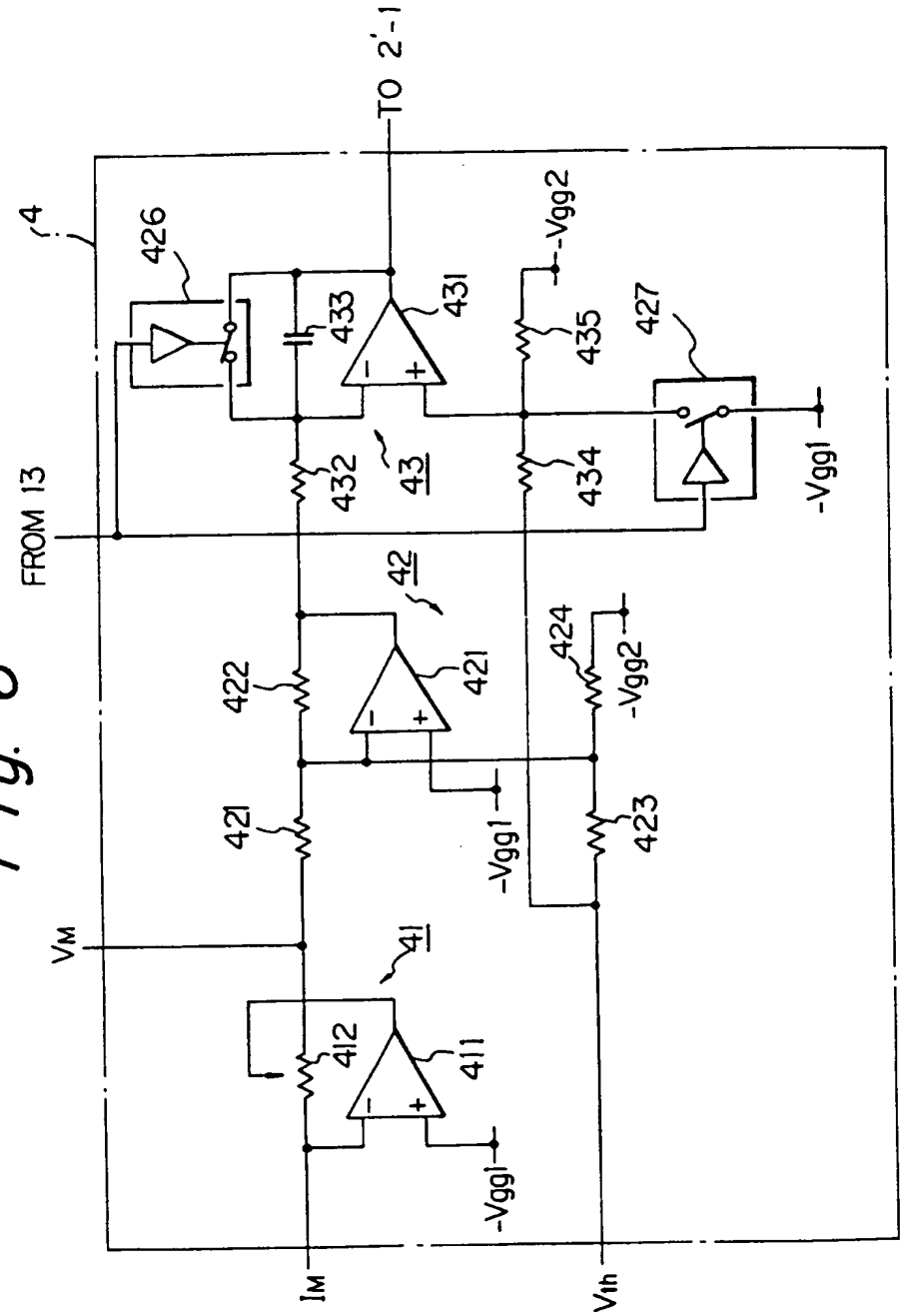

4
TO 2'-1
FROM 13
426
433
431
-Vgg2
435
427
432
43
434
-Vgg1
42
422
421
424
-Vgg2
421
-Vgg1
423
VM
41
412
411
-Vgg1
IM
Vth

Fig. 7

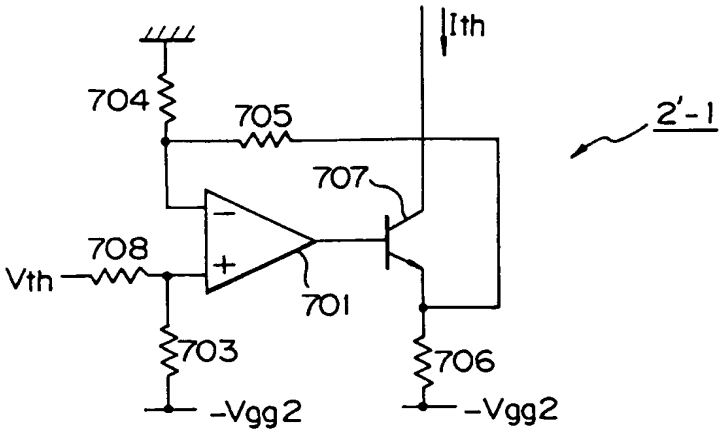

Ith
704
705
2'-1
707
708
Vth
701
703
706
-Vgg2
-Vgg2

Fig. 8

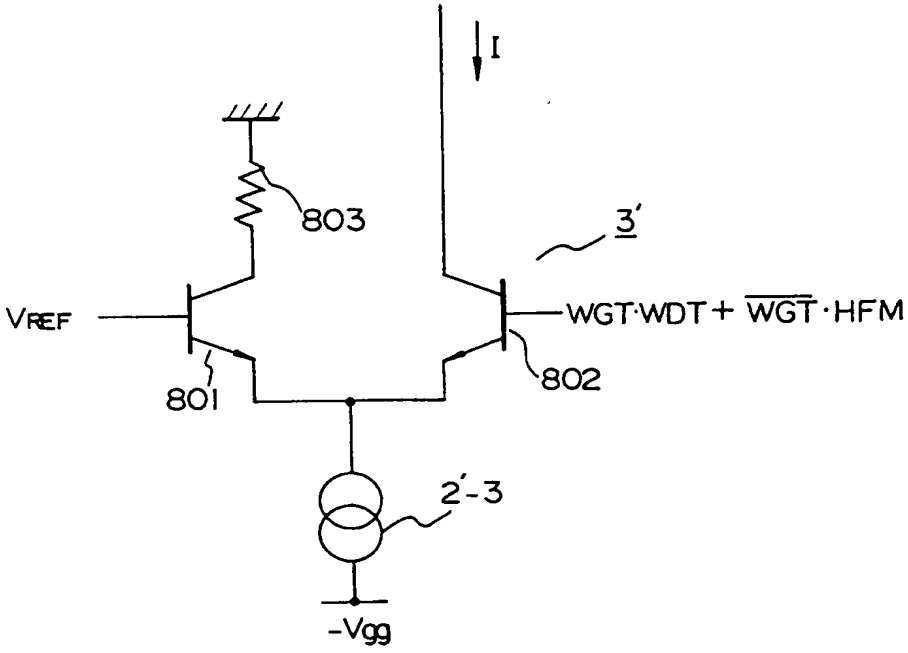

I
803
3'
VREF
WGT·WDT + $\overline{WGT}$·HFM
801
802
2'-3
-Vgg

Fig. 9

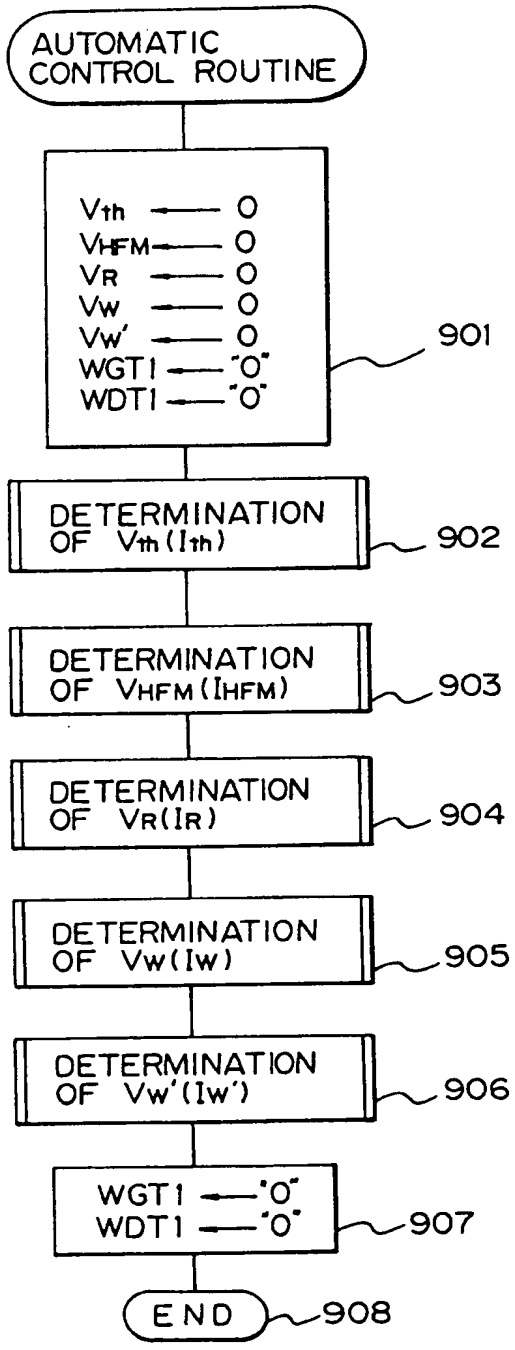

AUTOMATIC CONTROL ROUTINE
Vth ← 0
VHFM ← 0
VR ← 0
Vw ← 0
Vw' ← 0
WGT1 ← "0"
WDT1 ← "0"
901
DETERMINATION OF Vth (Ith)
902
DETERMINATION OF VHFM (IHFM)
903
DETERMINATION OF VR (IR)
904
DETERMINATION OF Vw (Iw)
905
DETERMINATION OF Vw' (Iw')
906
WGT1 ← "0"
WDT1 ← "0"
907
END
908

Fig. 10

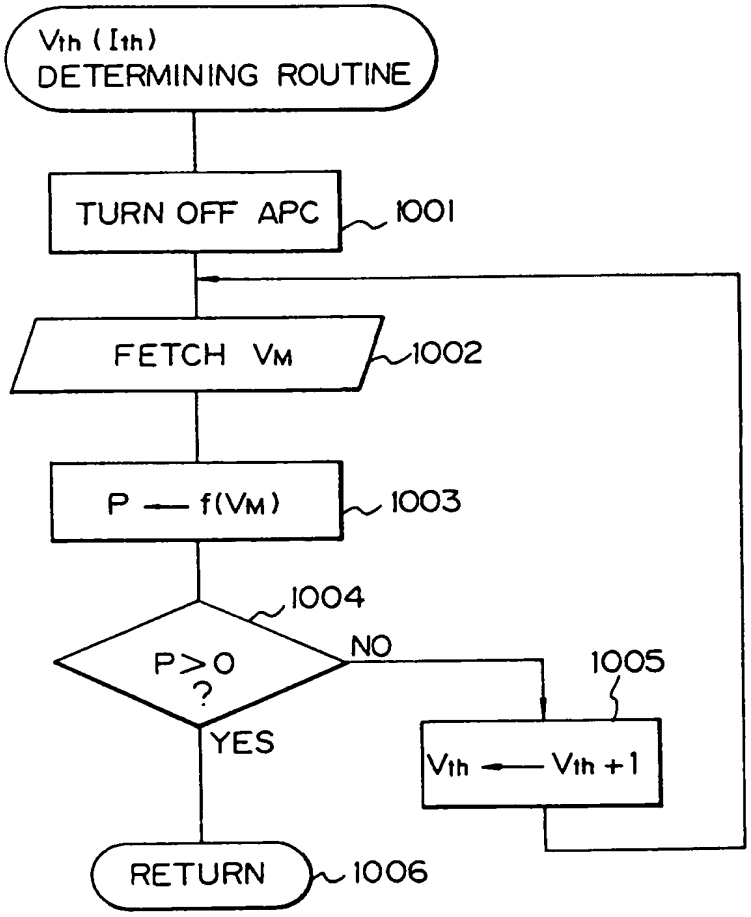

Vth (Ith)
DETERMINING ROUTINE
TURN OFF APC
1001
FETCH VM
1002
P — f(VM)
1003
1004
P>0
?
NO
YES
1005
Vth — Vth +1
RETURN
1006

Fig. 11

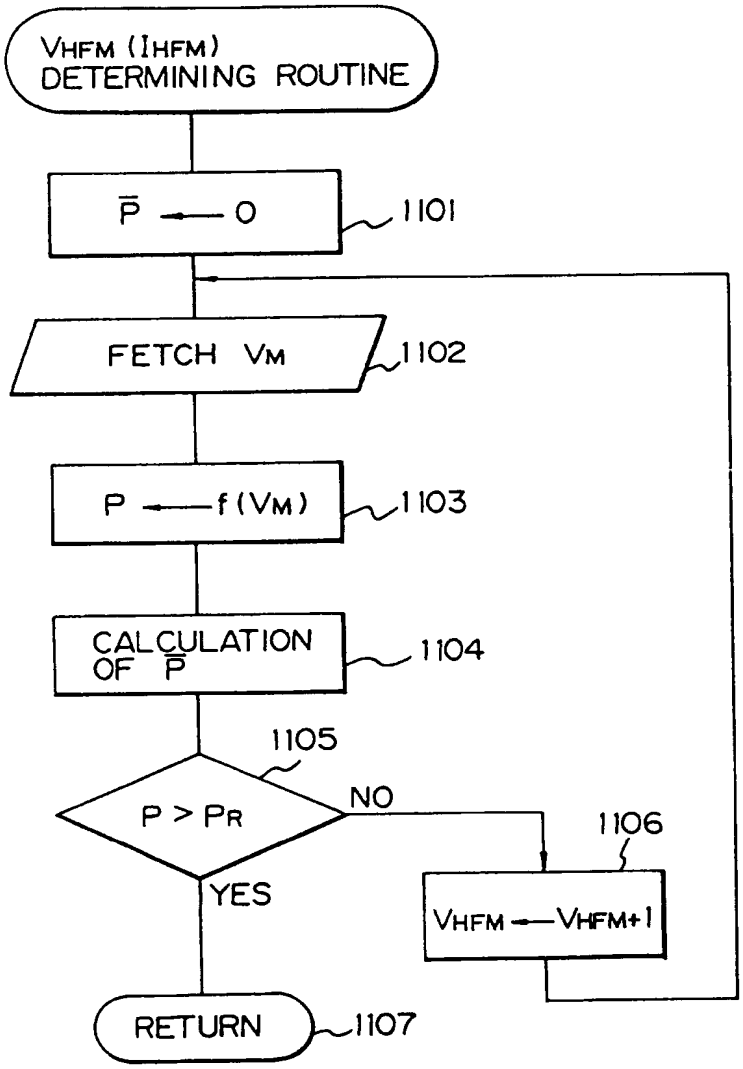

VHFM (IHFM) DETERMINING ROUTINE
P̄ ← 0
1101
FETCH VM
1102
P ← f(VM)
1103
CALCULATION OF P̄
1104
1105
P > PR
NO
YES
1106
VHFM ← VHFM+1
RETURN
1107

Fig. 12

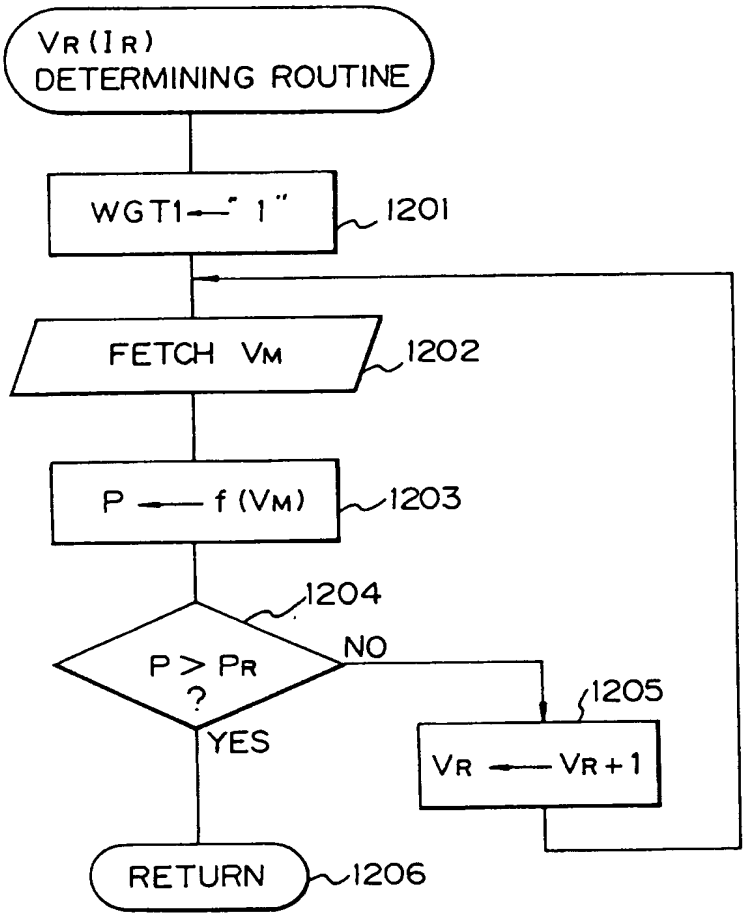

VR(IR)
DETERMINING ROUTINE
WGT1 ← "1"
1201
FETCH VM
1202
P ← f(VM)
1203
1204
P > PR ?
NO
YES
1205
VR ← VR+1
RETURN
1206

Fig. 13

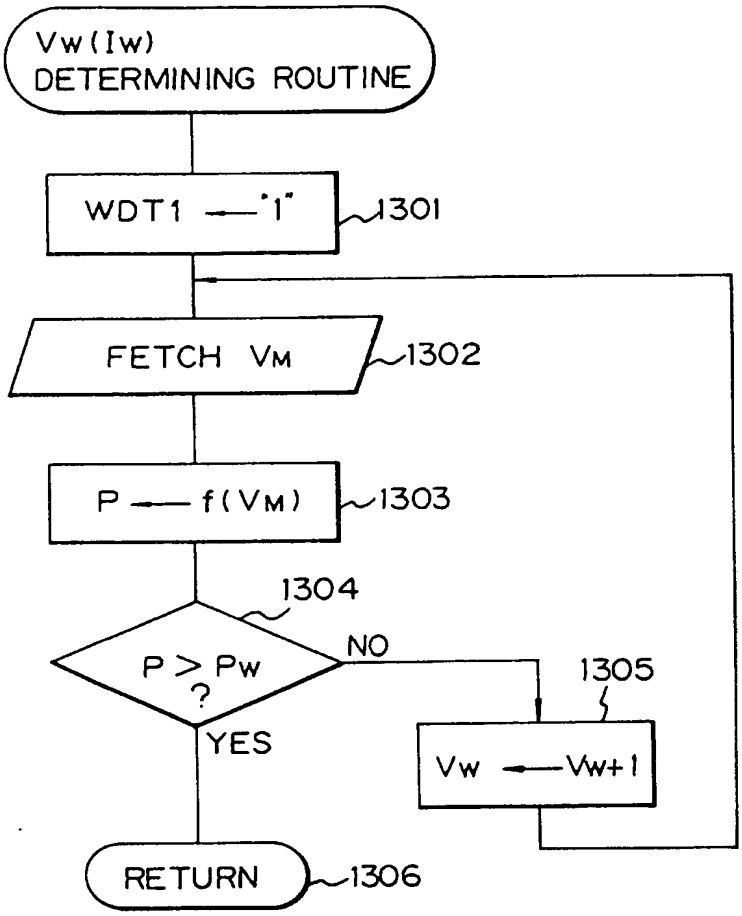
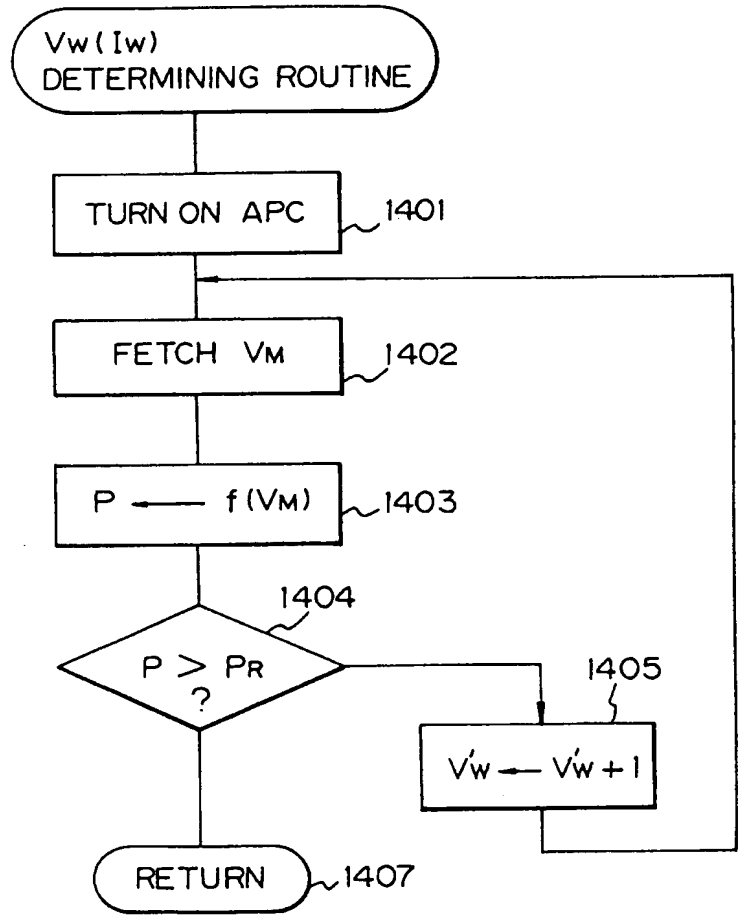

Vw(Iw)
DETERMINING ROUTINE
WDT1 ← "1"
1301
FETCH VM
1302
P ← f(VM)
1303
1304
P > Pw
?
NO
1305
YES
Vw ← Vw+1
RETURN
1306

Fig. 14


Vw(Iw)
DETERMINING ROUTINE
TURN ON APC
1401
FETCH VM
1402
P ← f(VM)
1403
1404
P > PR
?
1405
V'w ← V'w + 1
RETURN
1407

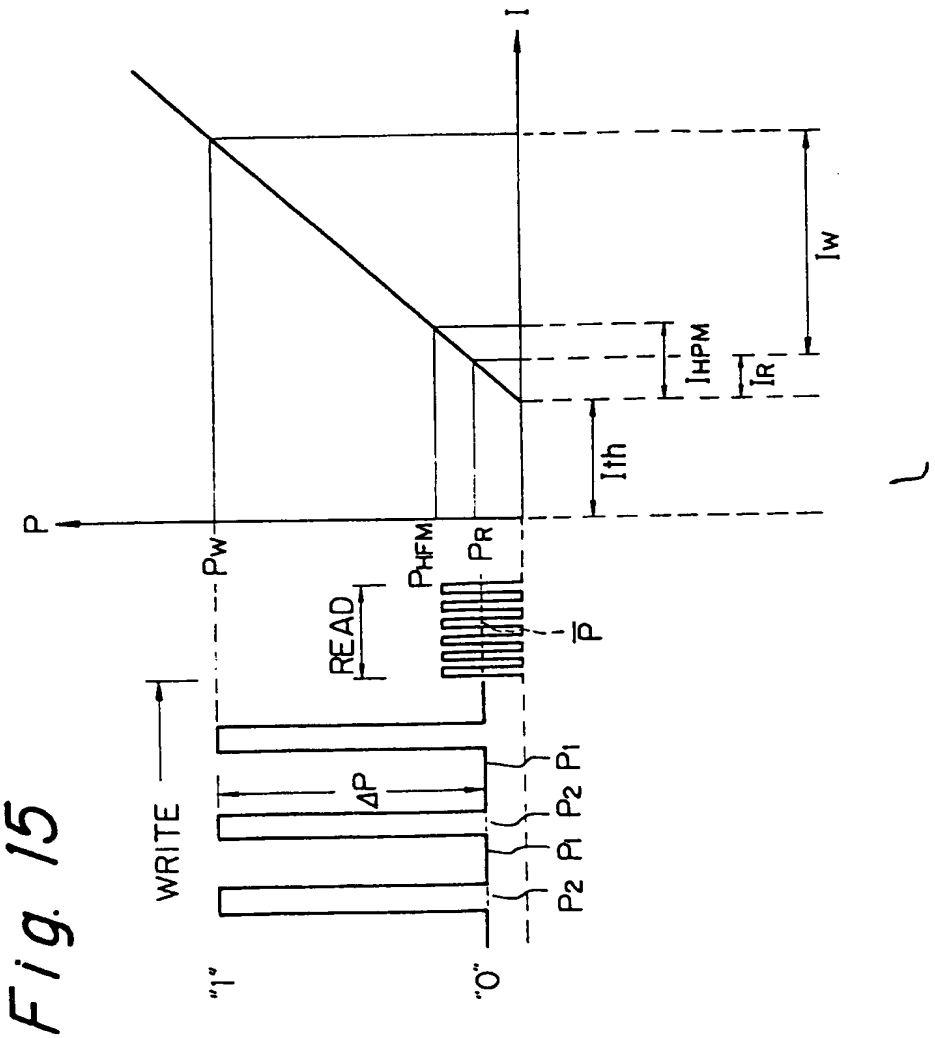


Fig. 15

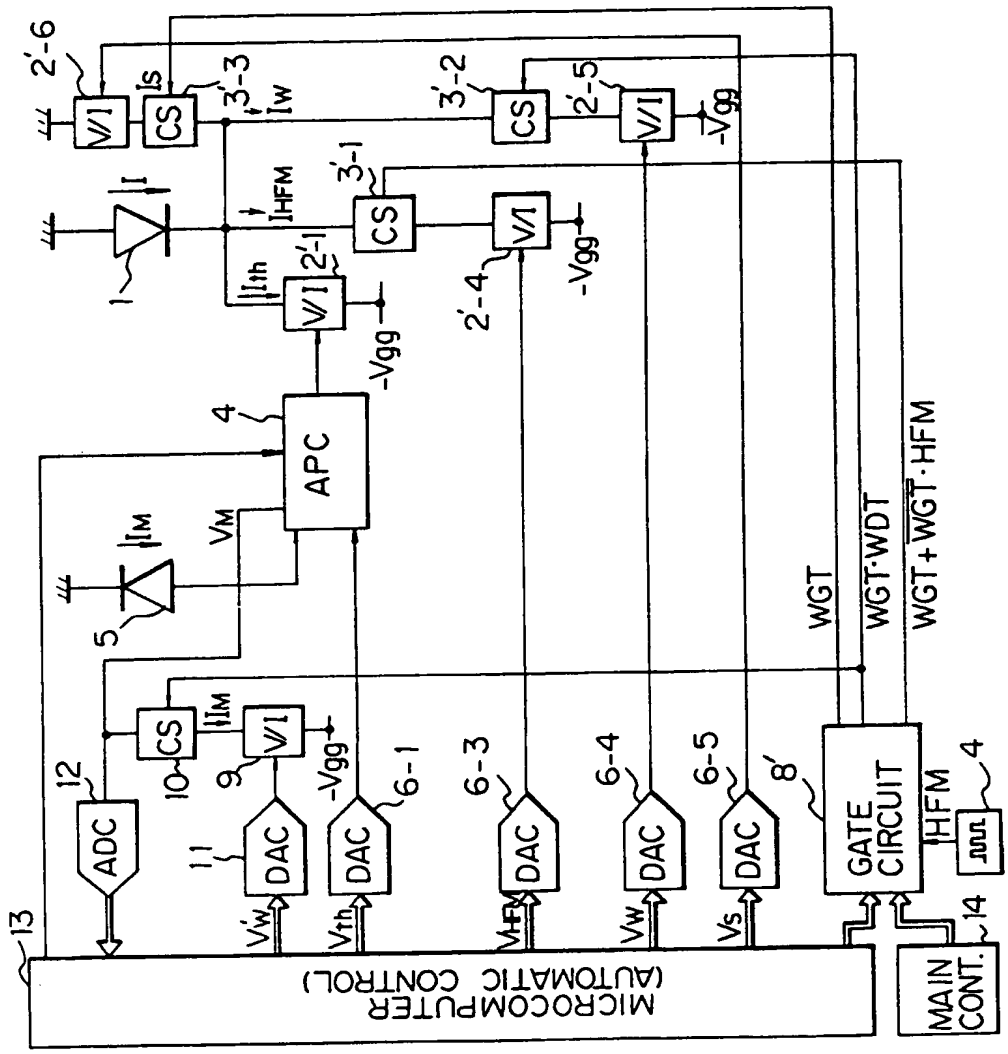

MICROCOMPUTER (AUTOMATIC CONTROL)
MAIN CONT.
GATE CIRCUIT
ADC
DAC
APC
CS
V/I
WGT
WGT·WDT
WGT + WGT·HFM
-Vgg

Fig. 16

Fig. 17

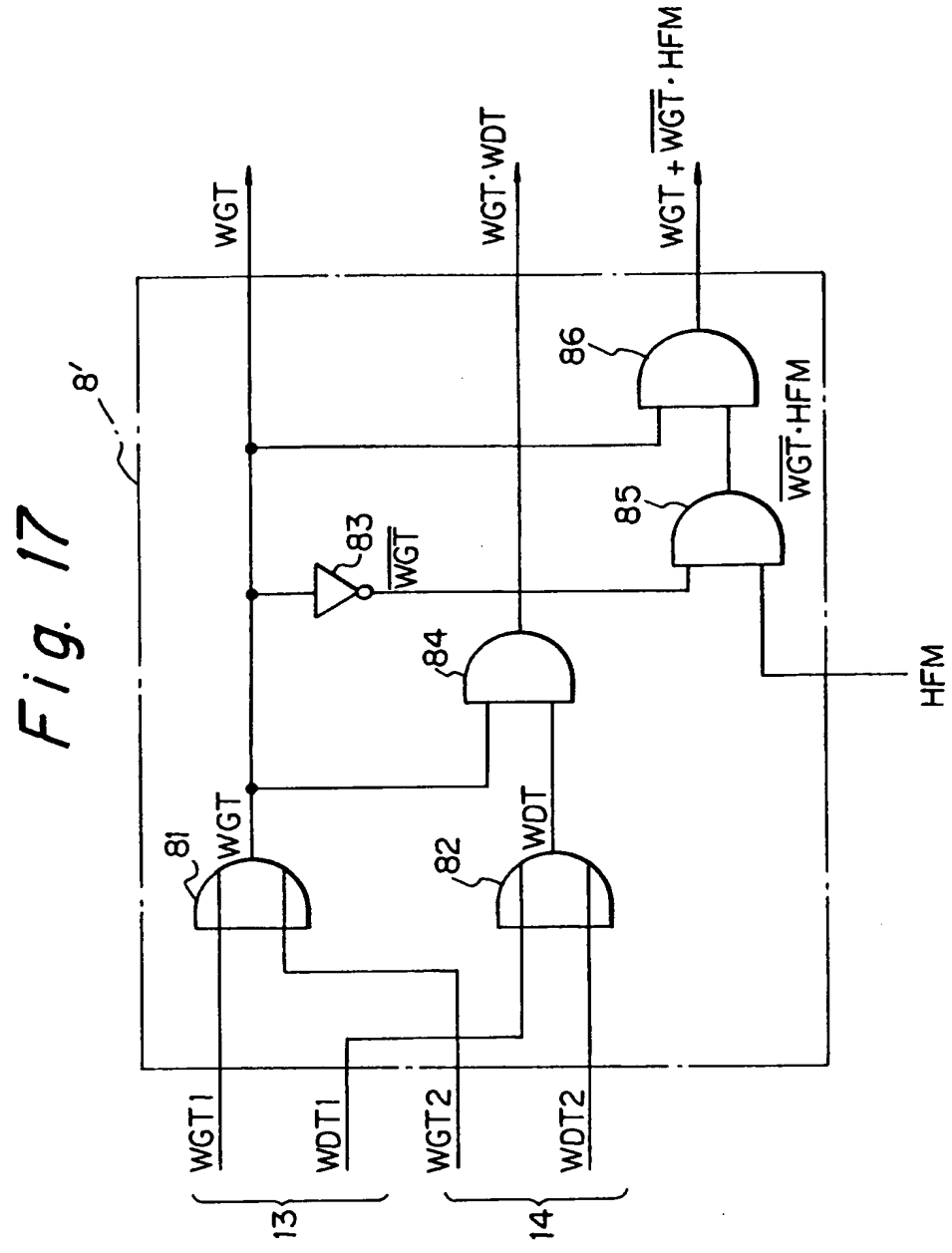

8'
WGT
WGT·WDT
WGT + $\overline{WGT}$·HFM
86
$\overline{WGT}$·HFM
85
83
$\overline{WGT}$
84
HFM
81
WGT
82
WDT
WGT1
WDT1
WGT2
WDT2
13
14

Fig. 18

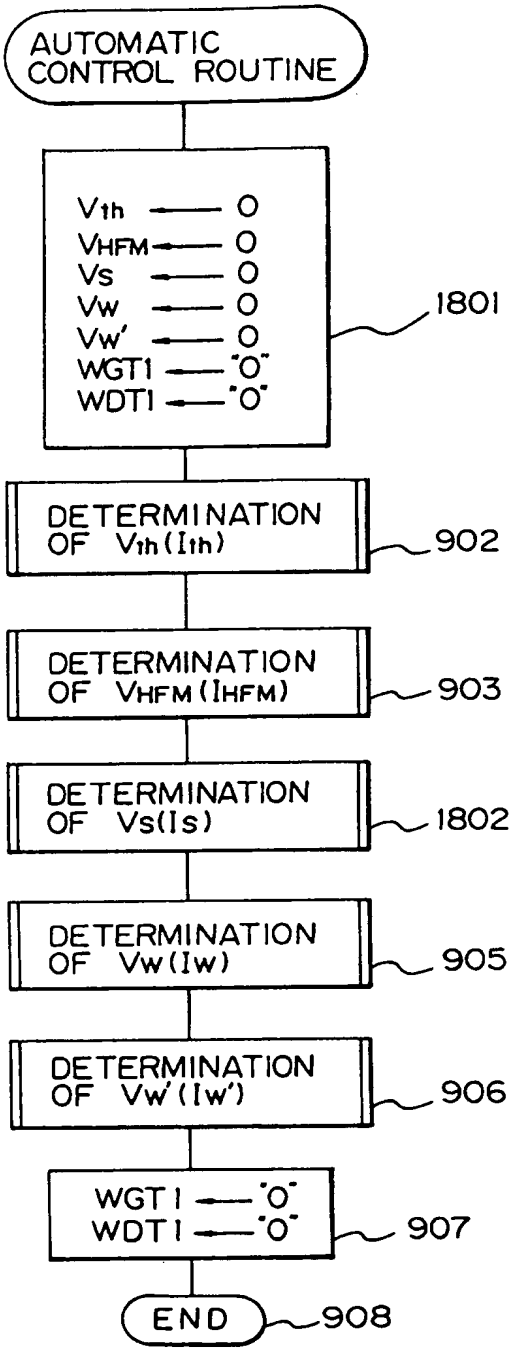

AUTOMATIC CONTROL ROUTINE
Vth — 0
VHFM — 0
Vs — 0
Vw — 0
Vw' — 0
WGT1 — "0"
WDT1 — "0"
1801
DETERMINATION OF Vth(Ith)
902
DETERMINATION OF VHFM(IHFM)
903
DETERMINATION OF Vs(Is)
1802
DETERMINATION OF Vw(Iw)
905
DETERMINATION OF Vw'(Iw')
906
WGT1 — "0"
WDT1 — "0"
907
END
908

Fig. 19

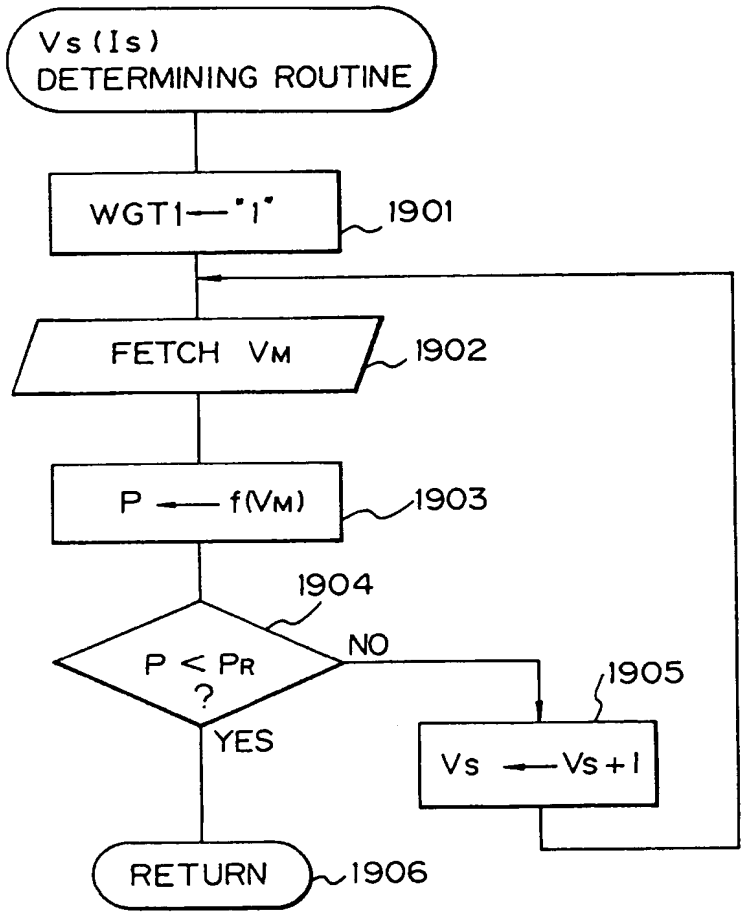
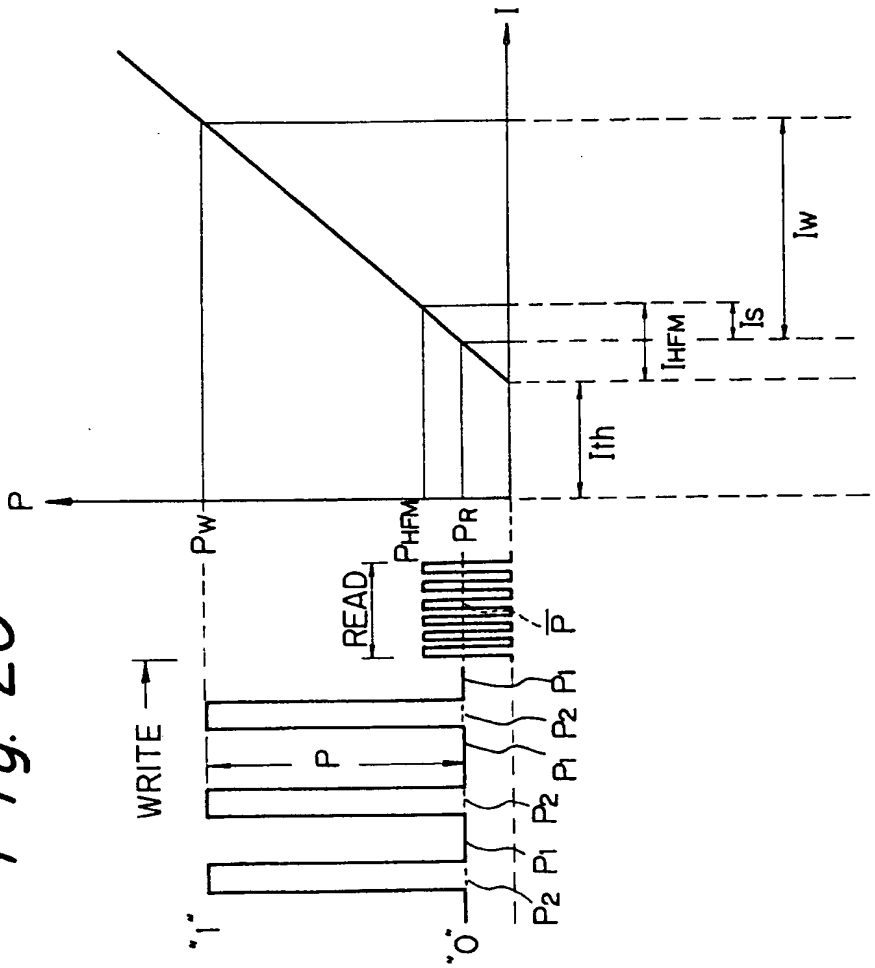

Vs (Is)
DETERMINING ROUTINE
WGT1 — "1"
1901
FETCH VM
1902
P ← f(VM)
1903
1904
P < PR
?
NO
YES
1905
Vs ← Vs + 1
RETURN
1906

Fig. 20


I
P
P_W
P_{HFM}
P_R
I_w
I_{HFM}
I_s
I_{th}
READ
$\overline{P}$
WRITE
P
"1"
"0"
P_1 P_2
P_1 P_2
P_1 P_2